



14.0 x 8.95 x 4.7 mm

3.3 Vdc • HCMOS/TTL • J-LEADED • PLASTIC MOLDED • SURFACE MOUNT
CRYSTAL CLOCK OSCILLATORS
ASML

FEATURES:

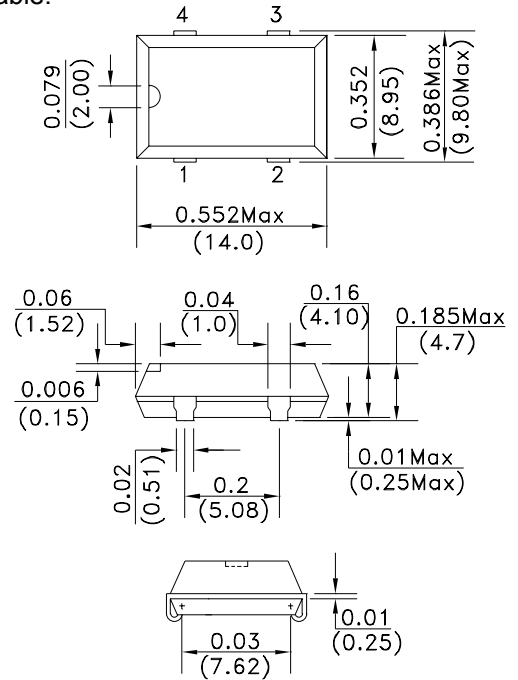
- Industry standard J-Leaded terminals.
- Low current consumption.
- HCMOS output.
- Extended temperature -40°C to +85°C option.
- Plastic molded SMD, Reflow capable.
- Tristate Enable/Disable.
- 3.3Vdc operation.

APPLICATIONS:

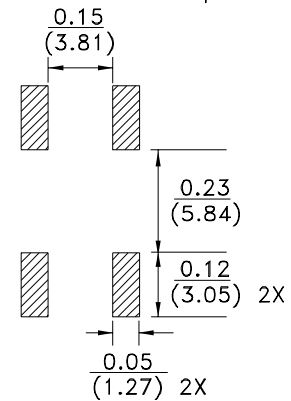
- Provide clock signals for microprocessors and digital circuits.
- Communication equipment, AV and OA equipment

STANDARD SPECIFICATIONS

PARAMETERS	SPECIFICATIONS
Frequency Range (F _O)	1MHz - 160MHz
Operating Temperature (T _{OPR})	0°C to +70°C (See Options)
Storage Temperature (T _{STO})	-40°C to +85°C
Frequency Stability (ΔF/F _O)	±100ppm max. (See Options)
Supply Voltage (V _{dd})	3.3Vdc ±10%
Input Current (I _{dd})	10mA max. (F ≤ 20MHz) ; 25mA max. (F ≤ 70MHz) 60mA max. (F ≤ 160MHz)
Duty Cycle or Symmetry	40 / 60% max. (See Options)
Rise and Fall Times (T _R / T _F)	6ns max.
Output Load	2TTL, 15pF max.
Output Voltage (V _{OH}) (V _{OL})	0.9 *V _{dd} min. 0.4Vdc max.
Start-up Time (T _{OSC})	10ms max.
Tristate Function (V _{IH}) (V _{IL})	"1" or Open: Oscillation ≥ 2.2V "0": (HiZ) < 0.6V Output disabled in high impedance
Aging	±5ppm/ Year max.



Recommended land pattern



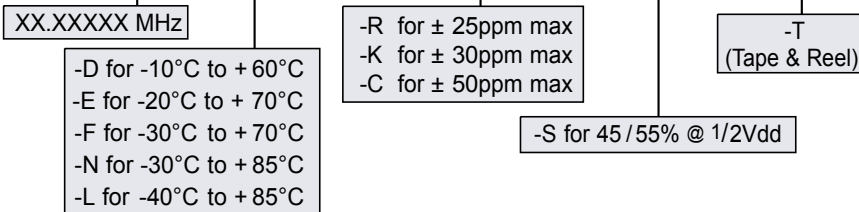
Dimensions: Inches (mm)

PIN NO.	FUNCTION
1	Tristate Enable
2	GND / Case
3	Output
4	V _{dd}

* Pin 1 has internal pull-up resistor which allows Pin 1 to be left floating (enable high)
 Test circuit, waveform, please see appendix B.
 Environmental and mechanical specifications, see appendix C. Group 2.
 Marking, see appendix G. Tape and Reel, see appendix H.(1,000 pcs./reel).
 A bypass capacitor 0.01 μF is required from V_{dd} to Gnd.
 Application notes, see appendix A. Reflow profile, see appendix E.

ORDERING OPTIONS

ASML - Frequency - Temperature - Frequency Stability - Duty Cycle - Packaging



NOTE: Left blank if standard • All specifications and markings subject to change without notice

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